

A multi-time-scale trigger to search for sub-millisecond burst phenomena.

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Abstract. Searching for extremely short GeV γ -ray bursts using atmospheric Cherenkov telescopes, requires a trigger that is sensitive on various time scales. In this paper we describe a digital trigger based on a reprogrammable gate array providing sensitivity in the time scales from $100ns$ to $10\mu s$. Such a system may find applications in a wide variety of research involving fast signals.

1 Introduction

In a very general way, small signal detection is usually limited in sensitivity by the noise. An efficient way to minimize noise effects, is to match the time scale sensitivity of the detector to the time scale of the signals being measured. In the particular case of Atmospheric Cherenkov Detectors, this principle has led to the intensive use of fast electronics with time scale of few nano-seconds (Barrau 1998) matching the time scales of the Cherenkov front produced by individual cosmic ray showers in the atmosphere. The improved sensitivity to Cherenkov pulses allowed the energy threshold for the detection of individual cosmic γ -rays to be lowered down to few hundred GeV and future detectors should reach below $100GeV$ (Weekes 1999, Hofmann 1997, Barrio 1998) achieving for the first time an overlap with detectors in space (Gehrels and Michelson 1999).

Even if Atmospheric Cherenkov detectors will remain insensitive to individual GeV- γ -rays, it has been shown(Krennrich 2000) that they can have a very competitive sensitivity to $E \geq 100MeV$ γ -ray bursts in a time domain mostly unexplored from $100ns$ to $10\mu s$. Those γ -rays are not detected individually but collectively. The cumulated Cherenkov light produced by the large number of showers reaches detectable levels. This is being explored in the Short Gamma Ray Front Air Cherenkov Experiment (SGARFACE) described in these proceedings (LeBohec 2001). In order to optimize the sensitivity on the time range to be covered, we have to apply

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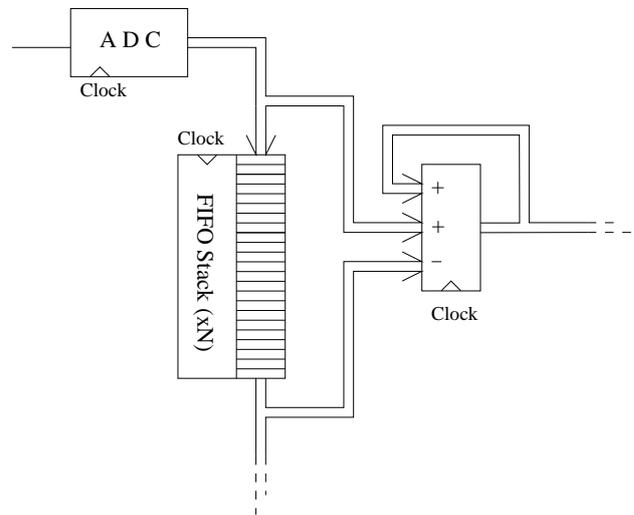


Fig. 1. Digital signal integration by summing the difference between the input and output of a FIFO stack.

the above principle for each possible signal duration. We also want to reduce the sensitivity to the very frequent short pulses due to individual cosmic ray showers. In this paper we present the multi-time-scale discriminator module that is currently being developed. We will first describe the digital signal processing. In the second part we will present how it is implemented.

2 The multi-time-scale trigger logic

The trigger decision must depend on the integrated signal over different time scales. After digitizing the signal at a rate of $\sim 50MHz$, it is possible to obtain the integral of the signal by constantly summing the difference between the values on the input and the output of a FIFO register stack as shown in figure 1. The time interval over which the signal is integrated simply is the number (N) of registers in the stack

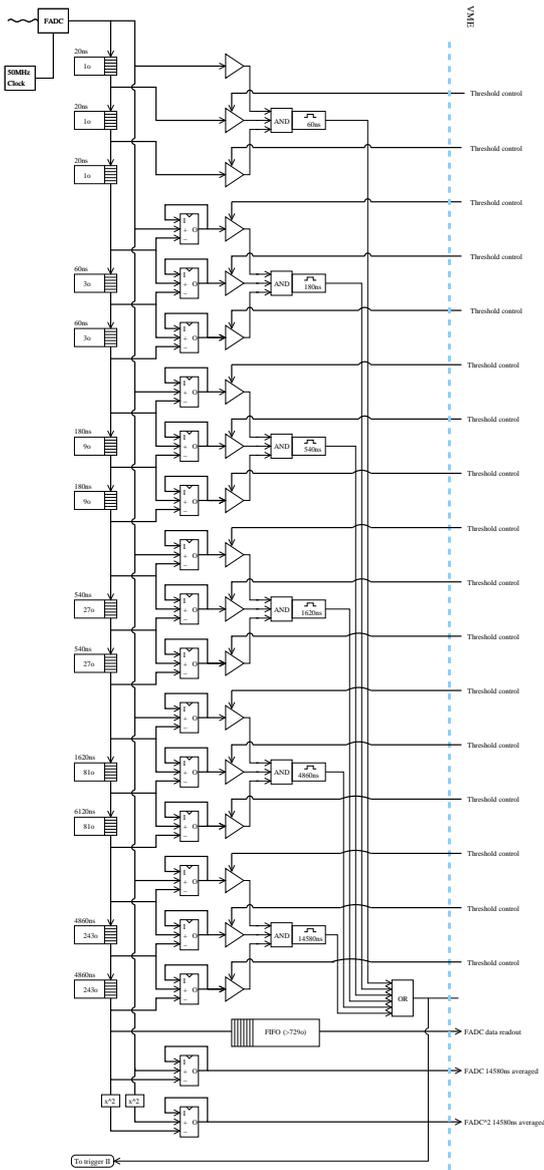


Fig. 2. Schematic for the integration and discrimination of the signal over three sectioned time windows in cascade.

multiplied by the time between successive signal samples acquisitions.

We could simply use a comparator on the summer output but the system would then be sensitive to both pulses with time scales comparable to the stack depth and very short pulse with large enough amplitudes. In order to avoid this inconvenience, we divide each time window in three subsections over which the signal is integrated. The trigger occurs when the three integral values are above a predefined threshold at the same time. This logic is replicated in cascade as shown in Figure 2 providing sensitivity over time windows of width 60ns, 180ns, 540ns, 1620ns, 4860ns and 14580ns.

Trigger signals from each time scale are given the corresponding width before being sent to an OR. The resulting signal will be sent to a coincidence unit which will issue

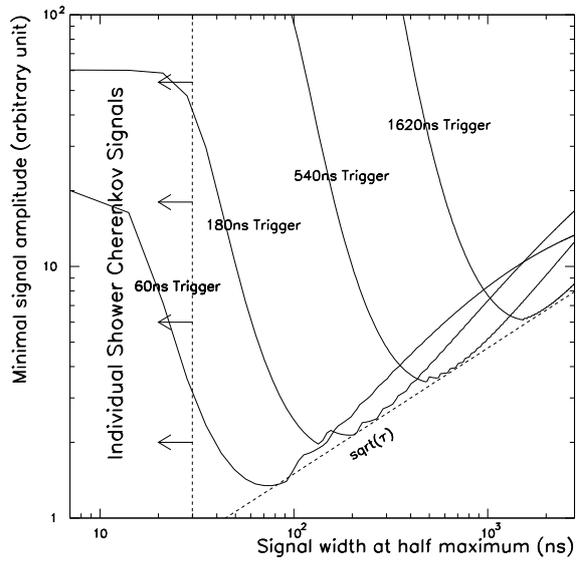


Fig. 3. Sensitivity provided by the discrimination on the integrated signal over each time scale as a function of the pulse width.

the global trigger of the acquisition of the sampled signals stored in the FIFO memories of each channel. The schematic also includes a calculation of the signal sample average and standard deviation which could be used in a dynamic control of the discrimination threshold applied to the different time scale integrals.

Figure 3 shows the sensitivity of the system as a function of the pulse width. For times larger than 80 nano-seconds the curve envelope remains close to \sqrt{time} as the threshold applied on the integrals were assumed to scale with the square root of the integration time. For times smaller than 60ns sensitivity is degraded by the requirement that at least 3 successive samples exceed the threshold simultaneously. Measurements with the Whipple telescope indicate that most pulses have a width of 15ns. Therefore, this trigger logic should provide a good protection against these signals. The residual sensitivity is in fact due to the bandwidth reduction which has to be applied to the analog signal before it is sampled and digitized at a 50MHz rate satisfying the Nyquist criterion in order to minimize the information loss.

3 Implementation with FPGA.

The SGARFACE experiment (LeBohec 2001), as operated on the Whipple telescope, will be based on 55 analog channels. The digitization and multi-time-scale discrimination of each channel will be performed by VME based modules with a multiplicity of 16 in such a way that 4 modules will be sufficient for the experiment. For all channels, the activity of each of the 6 different time-scale discriminators is displayed

by front panel LEDs mounted in 6 groups according to the time-scale they represent. The “OR” of the 6 time-scale discriminator signal is available at the front panel. These signals are collected by a coincidence unit that forms the global trigger signal of the experiment. The trigger signal is used to freeze the time register of a VME based GPS clock and stop the digitization in each multi-time-scale discriminator module. Digitization is resumed when the local computer (a VME base VMIC-7697 operated under QNX) has read the data from each channel.

The multi-time-scale discriminator circuit makes use of Xilinx and Actel Field Programmable Gate Arrays (FPGAs). The one Actel FPGA (Region Chip) is permanently programmed to work with Cypress VME chip set to provide VME interface for computer control and status reporting. This Region Chip interfaces with the local computer to report the circuit board identification and other status.

The digital signal processing shown in figure 2 is realised by a programmed Xilinx FPGA for each channel. All 16 Xilinx FPGA's are programmed from the local computer through the controlling Region Chip. This is a series of bytes written to the Xilinx FPGA that are both command and configuration data. The Xilinx FPGA's can also be cleared and reprogrammed using Region Chip circuits. When the Xilinx FPGAs have been programmed they can be addressed directly by the Cypress VME chip set and information can be sent to and received from the local computer through simple “*read*” and “*write*” commands. For example, each different time-scale discriminator threshold value is written to the Xilinx and can be read-back by the local computer for verification. After a trigger occurs the local computer can read out the stream of data present in the multi-time-scale discriminator logic in the Xilinx chip. The data stream is ready to resume with new data when the event data has been stored. The local computer can also write a diagnostic stream of data to any Xilinx FPGA to test for discriminator threshold and timing operations.

4 Conclusions

The first multi-time-scale discriminator module is being assembled at the time this paper is being written. The complexity of the logic that can be realized by the Xilinx chip is only limited by it's size which better has to be significantly larger than the minimum required in order to guaranty some freedom in the pin assignment as well as the possibility of evolution for the algorithm. A similar system with more than one digitized signal being sent to the same Xilinx chip could be used as a correlator on time scales as short as 20ns.

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